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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,244	05/25/2001	Norito Umehara	TIJ-28795	4574

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TEXAS INSTRUMENTS INCORPORATED  
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EXAMINER

ERDEM, FAZLI

ART UNIT PAPER NUMBER

2826

DATE MAILED: 08/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/866,244

Applicant(s)

UMEHARA ET AL.

Examiner

Fazli Erdem

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 May 2001.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-6 and 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell (6,373,141) in view of Hikita et al. (6,369,407) further in view of Wensel et al. (6,291,899).

Regarding Claims 1-7 and 11-17, Bell discloses an integrated circuit having wirebound pads suitable for probing where an integrated circuit device structure has probe pad extensions in electrical communication with the wire bond pads. The disclosure provides an improved probing system for wire bond packages such that neither the wire nor the wire bond from the pads on the chip surface need be removed during the testing procedure. The integrated circuit device includes a plurality of conductive pads having a first area for receiving a wire bond and a second area for receiving a wire bond and a second area for receiving a probe wherein the second area abuts, and is in electrical communication with the first area. Bell does not disclose a third region to be connected to external connection terminals and an encapsulation structure that fully encapsulated the chip and the conductor wires. However, Hikita et al. disclose a semiconductor device that has a substrate, an internal circuit formed on the semiconductor substrate, a connection pad formed on the semiconductor substrate and connected to the internal circuit, and a test pad formed on the semiconductor substrate as to be connected to the connection pad and used for functional testing of the internal. Test pads may be provided also to accompany

external connection pads that are connected to lead frames by wire bonding. Furthermore, Wensel et al. disclose a method and apparatus for reducing BGA warpage caused by encapsulation where the semiconductor chip and the conductor wires are fully encapsulated by and encapsulant.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include external pad connection structure and the encapsulation structure in Bell as taught by Hikita et al. and Wensel et al. respectively in order to connect the integrated circuit to external circuitry and in order to provide a better physical protection.

2. Claims 7-10, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell (6,249,675) in view of Hikita et al. (6,369,407) further in view of Wensel et al. (6,291,899).

Regarding Claims 8-10, 18 and 19, Bell discloses a structure and method for probing wiring bond pads. The disclosure provides an improved probing system and method for wire bond packages such that neither the wire nor the wire bond from the pads on the chip surface need be removed during the testing procedure. The integrated circuit device and the method includes a plurality of conductive pads having a first area for receiving a wire bond and a second area for receiving a wire bond and a second area for receiving a probe wherein the second area abuts, and is an electrical communication with the first area. Bell does not disclose a third region to be connected to external connection terminals and an encapsulation structure that fully encapsulated the chip and the conductor wires. However, Hikita et al. disclose a semiconductor device that has a substrate, an internal circuit formed on the semiconductor substrate, a connection pad formed on the semiconductor substrate and connected to the internal circuit, and

a test pad formed on the semiconductor substrate as to be connected to the connection pad and used for functional testing of the internal. Test pads may be provided also to accompany external connection pads that are connected to lead frames by wire bonding. Furthermore, Wensel et al. disclose a method and apparatus for reducing BGA warpage caused by encapsulation where the semiconductor chip and the conductor wires are fully encapsulated by and encapsulant.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include external pad connection structure and method of and the encapsulation structure and the method of in Bell as taught by Hikita et al. and Wensel et al. respectively in order to connect the integrated circuit to external circuitry and in order to provide a better physical protection.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (703) 305-3868. The examiner can normally be reached on M - F 8:00 - 5:00.

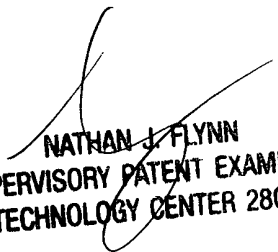
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Application/Control Number: 09/866,244  
Art Unit: 2826

Page 5

FE  
August 23, 2002



NATHAN J. FLYNN  
SUPERVISORY PATENT EXAMINER  
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